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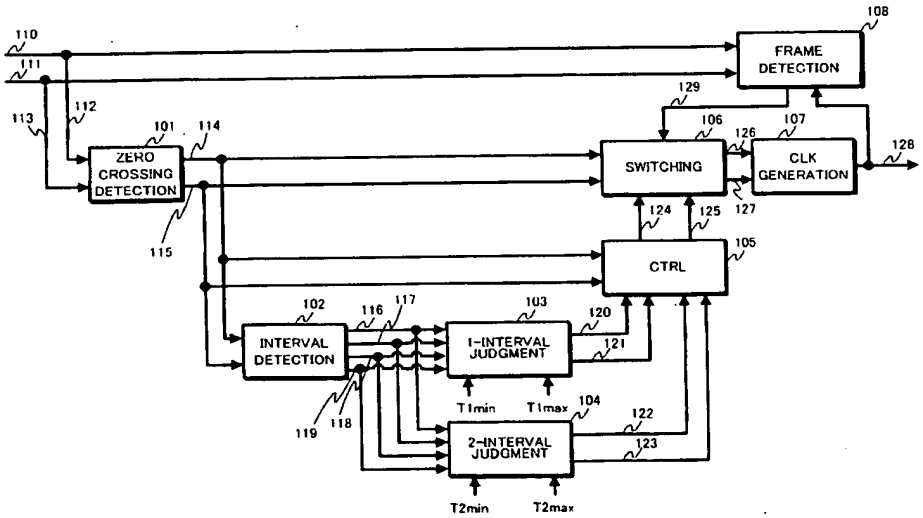
(54) Title: CLOCK RECOVERY CIRCUIT AND RECEIVER USING THE CIRCUIT



(57) Abstract: A clock recovery circuit capable of fast and accurate clock phase locking even in the presence of frequency shift and noise. The input signal includes, in order, a preamble with an alternating bit sequence pattern, a unique word and data. A detection unit detects zero crossings and measures the time interval therebetween. A 1-interval judgment unit judges whether an interval signal is within a predetermined range, and a 2-interval judgment unit sums two adjacent interval signals and judges whether the 2-interval signal is within a predetermined range. A control unit controls a zero-crossing signal based on the judgment result and outputs a valid zero-crossing signal if judged in the affirmative. A switching unit switches between outputting the zero-crossing signal and the valid zero-crossing signal as valid phase error information based on a frame reception signal input from a frame detection unit. A clock generation unit uses the valid phase error information in generating a symbol clock.

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